

1           1.    A method comprising:  
2                   forming a chalcogenide access device having a  
3   snapback voltage low enough to avoid disturbing data stored  
4   in a memory element while reading the memory element  
5   selected by the access device.

1           2.    The method of claim 1 including forming the  
2   chalcogenide access device to have a snapback voltage less  
3   than the threshold voltage of the memory element.

1           3.    The method of claim 2 including forming the  
2   memory element of a phase change material.

1           4.    The method of claim 2 including forming the  
2   memory element of a thin film material.

1           5.    The method of claim 1 including forming at least  
2   two arrays of memory elements stacked one on top of the  
3   other.

1           6.    The method of claim 5 including forming memory  
2   arrays with at least two memory elements each having a  
3   chalcogenide access device.

1           7.    The method of claim 6 including forming said  
2 chalcogenide access devices above a semiconductor  
3 substrate.

1           8.    The method of claim 7 including forming said  
2 memory elements above said semiconductor substrate.

1           9.    The method of claim 8 including forming an access  
2 device over a memory element.

1           10.   The method of claim 9 including forming the  
2 access device directly on top of the memory element without  
3 an intervening barrier layer.

1           11.   A memory comprising:  
2               a cell including a chalcogenide access device and  
3 a memory element, the chalcogenide access device having a  
4 snapback voltage low enough to avoid disturbing data stored  
5 in the memory element while reading the memory element.

1           12.   The memory of claim 11 wherein said chalcogenide  
2 access device has a snapback voltage less than the  
3 threshold voltage of the memory element.

1           13.   The memory of claim 12 wherein said memory  
2 element includes a phase change material.

1        14. The memory of claim 12 wherein said memory  
2 element includes a thin film material.

1        15. The memory of claim 11 including at least two  
2 memory arrays, each array including a plurality of cells  
3 stacked one on top of the other.

1        16. The memory of claim 15 including at least two  
2 memory elements each having a chalcogenide access device.

1        17. The memory of claim 16 including a semiconductor  
2 substrate, said chalcogenide access devices of said two  
3 memory elements formed above said semiconductor substrate.

1        18. The memory of claim 17 wherein said two memory  
2 elements are formed above said semiconductor substrate.

1        19. The memory of claim 18 including an access device  
2 located over at least one of the two memory elements.

1        20. The memory of claim 19 wherein the access device  
2 is directly on top of the memory element.

1        21. A system comprising:  
2            a processor-based device;

3           a wireless interface coupled to said processor-  
4 based device; and

5           a memory coupled to said device, said memory  
6 including a cell with a chalcogenide access device and a  
7 memory element, the chalcogenide access device having a  
8 snapback voltage low enough to avoid disturbing data stored  
9 in the memory element while reading the memory element.

1       22. The system of claim 21 wherein said chalcogenide  
2 access device has a snapback voltage less than the  
3 threshold voltage of the memory element.

1       23. The system of claim 22 wherein said memory  
2 element includes a phase change material.

1       24. The system of claim 21 wherein said memory  
2 includes at least two arrays each having rows and columns,  
3 one of said arrays stacked above the other of said arrays.

1       25. The system of claim 24 including two memory  
2 elements each having a chalcogenide access device.

1       26. The system of claim 25 including a substrate,  
2 said chalcogenide access devices formed above said  
3 substrate.

1        27. The system of claim 26 wherein said memory  
2 elements are formed above said semiconductor substrate.

1        28. The system of claim 27 including an access device  
2 located over the memory element.

1        29. The system of claim 28 wherein the access device  
2 is directly on top of the memory element.

1        30. The system of claim 21 wherein said access device  
2 and said memory element include chalcogenide material and  
3 the chalcogenide material used in the access device and the  
4 memory element are different chalcogenide materials.

1        31. The system of claim 21 wherein said wireless  
2 interface includes a dipole antenna.